drain, and a metallic source contact coupled to the source and to the epitaxial layer to form a Schottky diode, comprising diverting current from the source of the DMOS transistor with the Schottky diode that is co-integrated with the DMOS transistor when the source becomes more positive than a drain of the DMOS transistor.

REMARKS

Claims 17-20 are presented for further examination. Claim 17 has been amended.

In the Office Action dated October 24, 2001, the Examiner rejected claims 17, 19, and 20 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 4,811,065 ("Cogan"). Claim 18 was rejected under 35 U.S.C. §103(a) as unpatentable over Cogan in view of European Patent 0747969 ("Pearce").

Applicant respectfully disagrees with the bases for the rejections and requests reconsideration and further examination of the claims.

The present invention is directed to a method of operating a DMOS transistor having a Schottky diode co-integrated therewith. The DMOS transistor is in the form of that disclosed and claimed in U.S. Patent No. 5,925,910, which is the parent of the present application. As disclosed and claimed therein, the DMOS transistor has a drain of first conductivity formed in an epitaxial layer of same conductivity, a body formed of second conductivity in the epitaxial layer, a source of first conductivity in the body, a gate electrode positioned above the source, the body, and the epitaxial layer, a conductive contact coupled to the drain, and a metallic source contact coupled to the source and to the epitaxial layer to form a Schottky diode. The method of operation includes diverting current from the source of the DMOS transistor with the Schottky diode when the DMOS transistor source becomes more positive than the drain of the DMOS transistor. Preferably, the act of diverting current from the source of the DMOS transistor includes diverting current from a parasitic bipolar transistor having a collector coupled to a substrate in which both the DMOS transistor and the Schottky diode are integrated.

Cogan, U.S. Patent No. 4,811,065, does not disclose or suggest a DMOS transistor having the construction and method of operation as recited in the disclosed and claimed embodiments of the invention. This is acknowledged by the Office in the allowance of claims

drawn to the recited DMOS transistor in the parent application of the present application, which is now issued U.S. Patent No. 5,925,910. More particularly, the Examiner's attention is drawn to independent claim 9 which recites essentially the same structure as disclosed and claimed in the present application.

Turning to the claims, independent claim 17 is directed to a method of operating a DMOS transistor having a drain of first conductivity formed in an expitaxial layer of same conductivity, a body formed of second conductivity in the epitaxial layer, a source of first conductivity in the body, a gate electrode positioned above the source, the body, and epitaxial layer, a conductive contact coupled to the drain, and a metallic source contact coupled to the source and the epitaxial layer to form a Schottky diode. Claim 17 further recites the method as comprising diverting current from the source of the DMOS transistor with the Schottky diode that is co-integrated therewith when the source of the DMOS transistor becomes more positive than a drain of a DMOS transistor. Nowhere does Cogan teach or suggest using a DMOS transistor of the construction recited in claim 17 in the manner and method as recited therein. Applicants respectfully submit that claim 17 is allowable for these reasons.

Dependent claims 18-20 are directed to additional embodiments of the invention. Claim 18, for example, recites diverting current from a parasitic bipolar transistor having a collector coupled to a substrate in which both the DMOS transistor and the Schottky diode are integrated. As the Examiner acknowledges, nowhere does Cogan teach or suggest such a method. For this missing element, the Examiner cites Pearce, European Patent 0747969. However, applicant is unable to find any teaching in Pearce that provides the missing element of diverting current from a parasitic bipolar transistor having a collector coupled to a substrate in which both a DMOS transistor and a Schottky diode are integrated. Any combination of Pearce with Cogan would clearly fall short of the combination recited in claim 18. Applicants respectfully submit that dependent claims 18-20 are allowable for the reasons set forth above as well as for the reasons why claim 17 is allowable.

In the event the Examiner finds minor informalities, the Examiner is urged to contact applicant's undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version With Markings to Show Changes Made.**"

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claim 17 has been amended as follows:

17. (Amended) A method of operating a DMOS transistor having a drain of first conductivity formed in an expitaxial layer of same conductivity, a body formed of second conductivity in the epitaxial layer, a source of first conductivity in the body, a gate electrode positioned above the source, the body, and the epitaxial layer, a conductive contact coupled to the drain, and a metallic source contact coupled to the source and to the epitaxial layer to form a Schottky diode, comprising diverting current from ~~a~~ the source of the DMOS transistor with ~~a~~ the Schottky diode that is co-integrated with the DMOS transistor when the source becomes more positive than a drain of the DMOS transistor.

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